128-Channel Serial to Parallel Converter with Push-Pull Outputs

Features

- Processed with HVCMOS technology
- 128 Channels
- 4 Separate shift registers
- 5V CMOS logic
- Output voltages up to 80V
- ±30mA output current capability
- Low power level shifting
- 40MHz data shifting
- Latched data outputs
- Forward and reverse shifting option via DIR pin
- Output diode to ground and V_{PP} for efficient power recovery
- Outputs can be hot switched

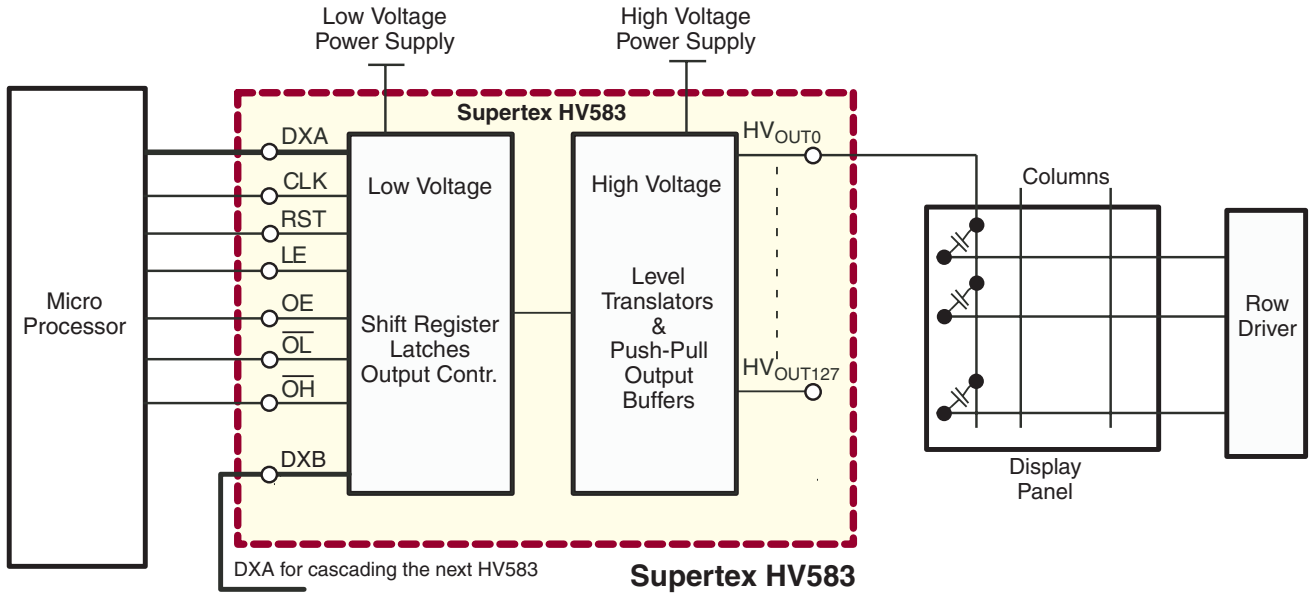
General Description

The Supertex HV583 is a 128-channel low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a display driver. It can also be used in any application requiring multiple output, high voltage current sourcing and sinking capability such as plasma displays and inkjet printers. The device has 4 parallel 32-bit shift registers, permitting data rates 4X the speed of one. The data are shifted in during the low to high clock transition. There are also 128 latches and control logic to shift clockwise or counterclockwise. High at RST input pin clears contents of both: the shift register and the latch. The outputs can be in a high impedance state via the output enable logic pin.

Applications

- Plasma Displays
- Inkjet Printers

Typical Application



Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options
		Die
HV583	80V	HV583X

Absolute Maximum Ratings*

V_{PP}, High voltage supply	-0.5V to +90V
V_{DD}, Logic supply voltage	-0.5V to +7.0V
I_{OUT}, Output source and sink current	-65mA to +40mA
I_{DIODE}, Output body diode current	-65mA to +65mA
Logic input voltages	-0.5V to V_{DD}+0.5V
Tj, Junction temperature	-25°C to +150°C
Storage temperature	-40°C to +150°C

**All voltages are referenced to device ground. Absolute maximum ratings are those values which damage to the device may occur. Functional operation under these conditions is not implied. Continous operation of the device at the absolute rating level may affect device reliability.*

Notes:

Power-up sequence should be the following:

1. *Connect ground.*
2. *Apply V_{DD}.*
3. *Set all inputs (Data, CLK, etc.) to a known state.*
4. *Apply V_{PP}.*

Power-down sequence should be the reverse of the above.

Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{PP}	High voltage supply	15		80	V	Cload = 300pF
V_{DD}	Low voltage supply	4.5	5.0	5.5	V	
I_{OUT}	HVout peak output current	-30		30	mA	
SR	V_{PP} power supply slew rate			8.0	V/µs	
f_{CLK}	Clock frequency			40	MHz	Data read
				25	MHz	Cascade connection
Tj	Operating junction temperature	-25		+125	°C	

Electrical Characteristics

DC Characteristics *(Tj = 25°C, V_{DD} = 5V, V_{PP} = 80V)*

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{PPQ}	V_{PP} quiescent supply current			10	µA	
I_{DDQ}	V_{DD} quiescent supply current			10	µA	
HV_{OH}	High level output voltage	73	76		V	I_{OUT} = 30mA, V_{PP} = 80V
		10				I_{OUT} = 10mA, V_{PP} = 20V
HV_{OHD}	Output p-channel body diode			81.5	V	I_{OUT} = -30mA, V_{PP} =80V
HV_{OL}	Low level output voltage		3.0	6.0	V	I_{OUT} = -30mA
HV_{OLD}	Output n-channel body diode	-1.5			V	I_{OUT} = +30mA
V_{IH}	Logic input high voltage	2.0		V_{DD}	V	V_{DD} = 4.5V to 5.5V
V_{IL}	Logic input low voltage	0		0.8	V	V_{DD} = 4.5V to 5.5V
I_{IH}	Logic input high current			1.0	µA	V_{IH} = 5.3V, V_{DD} = 5.0V
		10	30	50	µA	V_{IH} = 5.0V, For DIR only
I_{IL}	Logic input low current	-1.0			µA	V_{IL} = -0.3V
V_{OH}	Logic output high	4.5V			V	I_{OUT} = 1.0mA
V_{OL}	Logic output low			0.5V	V	I_{OUT} = -1.0mA

AC Electrical Characteristics *(Tj = 25°C, V_{DD} = 5V, V_{PP} = 80V)*

Symbol	Parameter	Min	Typ	Max	Units	Conditions
twCLK	Clock pulse width, high and low	10			ns	V_{DD} =4.5V to 5.5V, Tj=-25°C to 125°C
twLE	LE pulse width, high and low	10			ns	
tsu1	Setup time, DXAs, DXBs to CLK	5			ns	
tsu2	Setup time, CLK to LE	10			ns	
tsu3	Setup time, LE to $\overline{OL}$, $\overline{OH}$	25			ns	
th1	Hold time, CLK to DXAs, DXBs	5			ns	
th2	Hold time, LE to CLK	10			ns	
tpdHL	CLK to DXAs, DXBs			25	ns	C=15pF
tpdLH	CLK to DXAs, DXBs			25	ns	C=15pF
tpHL	LE, $\overline{OH}$, $\overline{OL}$ to HV_{OUT}			150	ns	C=50pF
tpLH	LE, $\overline{OH}$, $\overline{OL}$ to HV_{OUT}	Typ -20	tpHL+tf	Typ +40	ns	C=80pF
tpHZL	OE to HV_{OUT}			150	ns	C=50pF
tpLZH	OE to HV_{OUT}	Typ -20	tpHL+tf	Typ +40	ns	C=80pF
tpHZ	OE to HV_{OUT}			300	ns	Rl=10K, C=50pF
tpLZ	OE to HV_{OUT}			300	ns	Rl=10K, C=50pF
tr	HV_{OUT}			120	ns	C=50pF
tf	HV_{OUT}			120	ns	C=50pF

Shift Register Truth Table

DIR	CLK	State of Shift Register	Shift Direction
L or open	L to H	Shift	D_{XB} to D_{XA}
L or open	H to L	Hold	D_{XB} to D_{XA}
H	L to H	Shift	D_{XA} to D_{XB}
H	H to L	Hold	D_{XA} to D_{XB}

Latch Truth Table

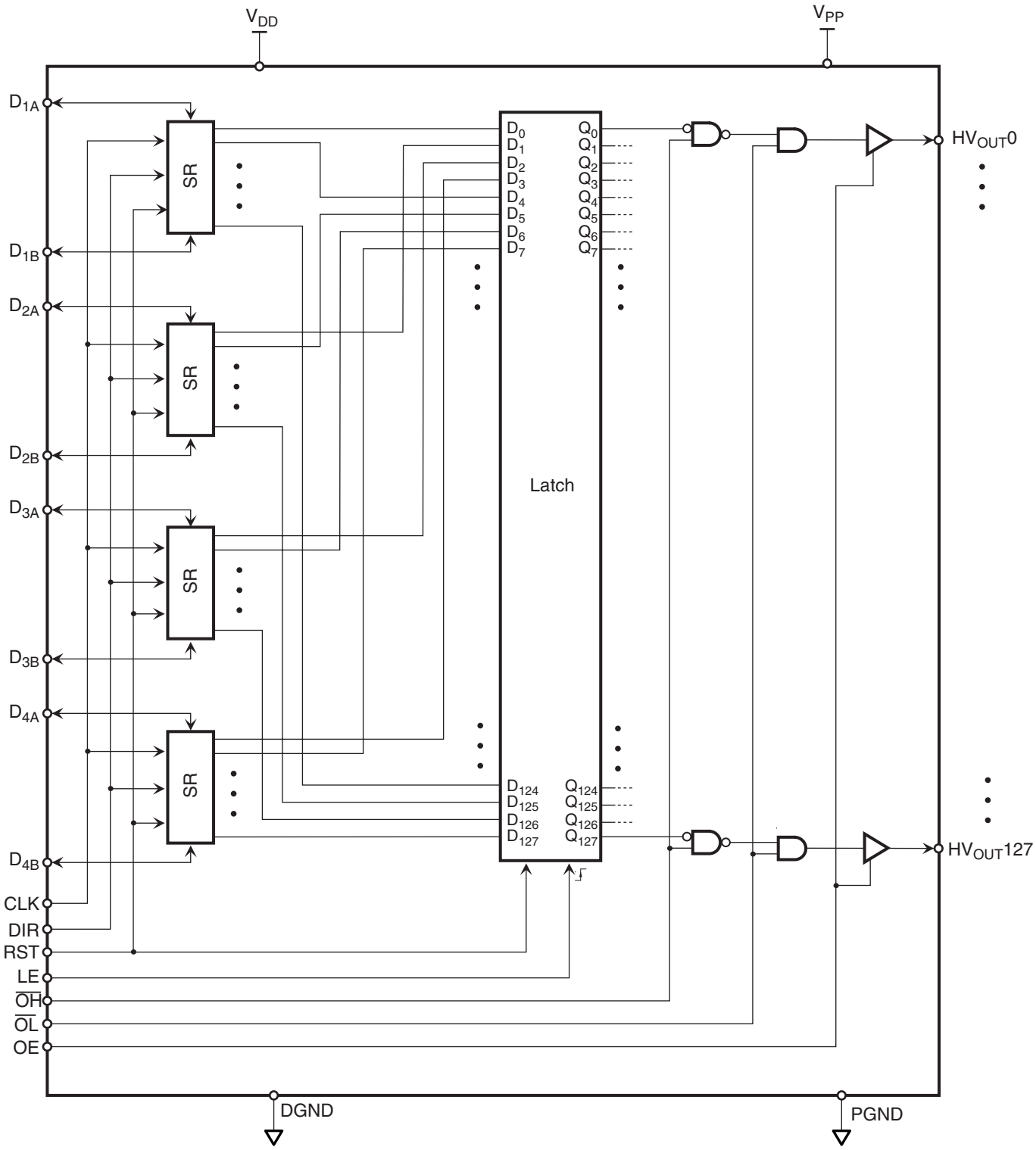
LE	Output State of Latch
L to H	Latch execution
H to L	Hold

HV_{OUT} Truth Table

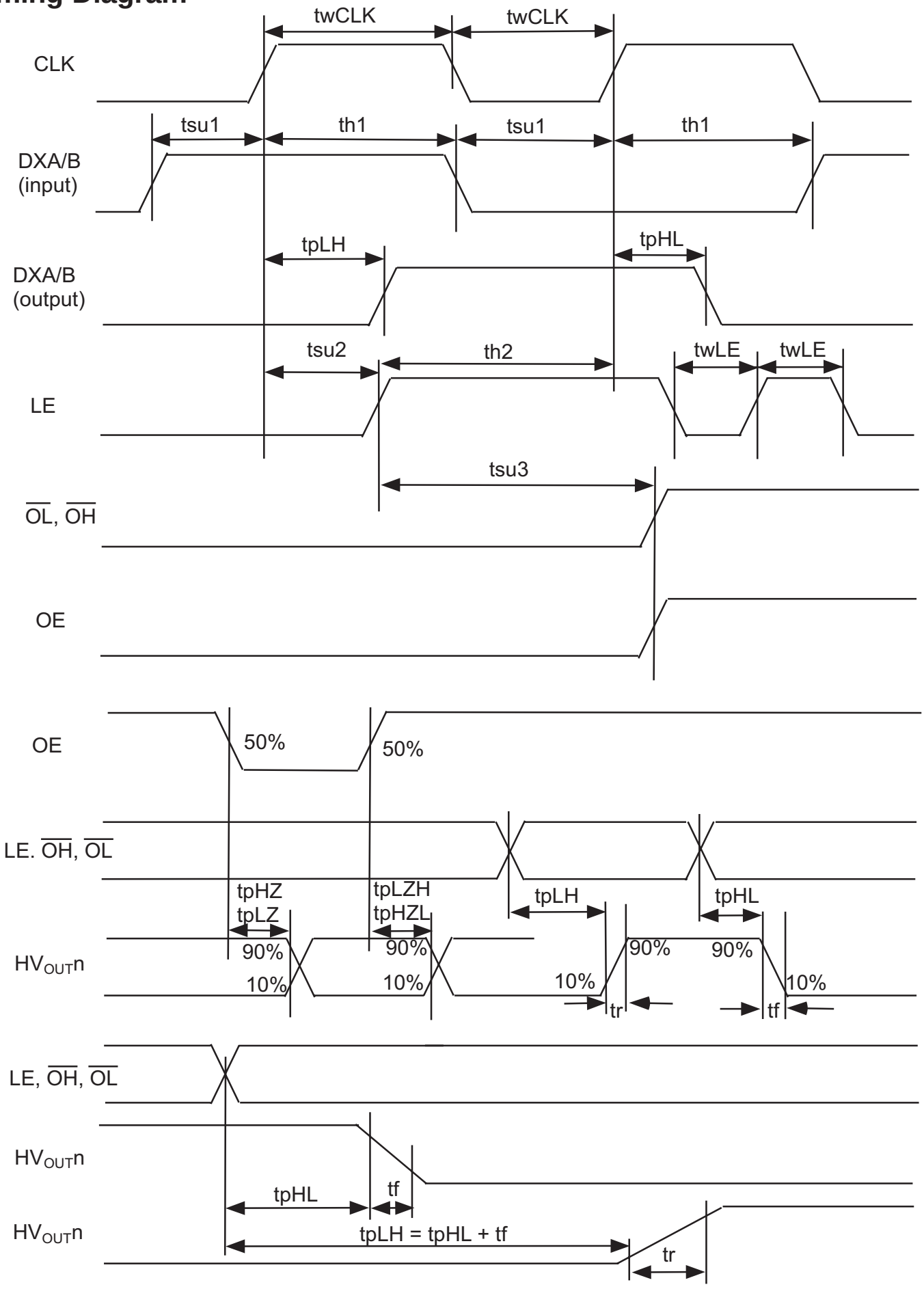
OE	$\overline{OL}$	$\overline{OH}$	DXA/DXB	HV_{OUT}
L	X	X	X	Z
H	L	X	X	L
H	H	L	X	H
H	H	H	L	L
H	H	H	H	H

H = Level High
L = Level Low
X = Don't care. Can be High or Low
Z = High impedance. Open circuit.

Block Diagram



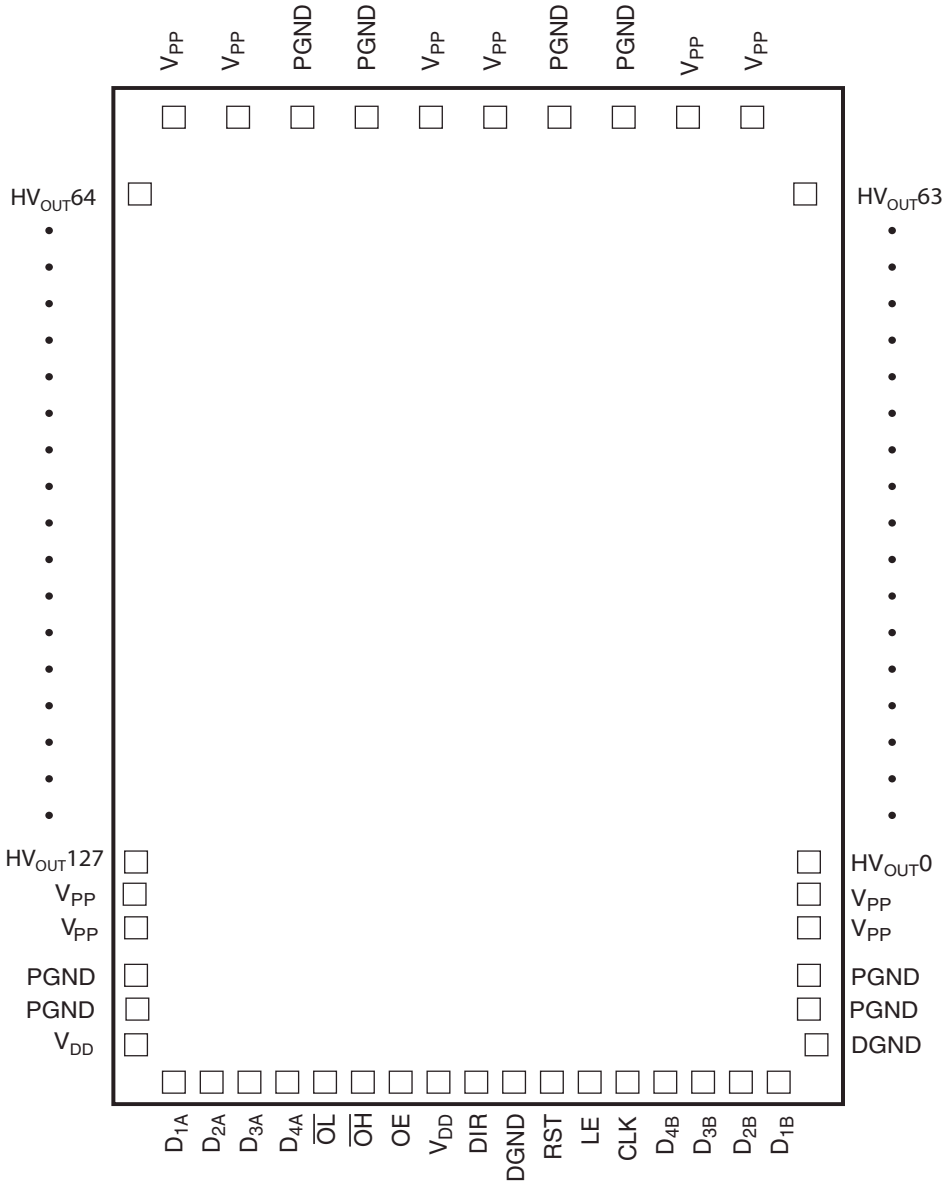
Timing Diagram



Pad Description

V_{PP}	High voltage supply for outputs.
V_{DD}	Low voltage logic supply
D1A to D4A	Right data input/output. Input when Dir = H, Output when Dir = L.
D1B to D4B	Left data input/output. Input when Dir = L, Output when Dir = H.
Dir	Dir = L or open, D_{XB} to D_{XA} shift. Dir = H, D_{XA} to D_{XB} shift.
CLK	Clock input. Data shifted from low to high transition.
RST	Resets latches.
LE	Latch enable. Data latches during rising edge LE.
OE	Output enable. HV_{OUT} high impedance control.
$\overline{OL}$	Output low bar. All HV_{OUT} = low when this pin is low.
$\overline{OH}$	OH bar input. All HV_{OUT} = high when this pin is low.
DGND	Digital logic ground.
PGND	HV_{OUT} output ground.
$HV_{OUT}0$ to $HV_{OUT}127$	High voltage outputs.

Pad Location



Pad Coordinates

Pad #	Name	X	Y
1	V_{DD}	0	0
2	PGND	0	150
3	PGND	0	260
4	V_{PP}	0	410
5	V_{PP}	0	520
6	$HV_{OUT}127$	0	670
7	$HV_{OUT}126$	0	780
8	$HV_{OUT}125$	0	890
9	$HV_{OUT}124$	0	1000
10	$HV_{OUT}123$	0	1110
11	$HV_{OUT}122$	0	1220
12	$HV_{OUT}121$	0	1330
13	$HV_{OUT}120$	0	1440
14	$HV_{OUT}119$	0	1550
15	$HV_{OUT}118$	0	1660
16	$HV_{OUT}117$	0	1770
17	$HV_{OUT}116$	0	1880
18	$HV_{OUT}115$	0	1990
19	$HV_{OUT}114$	0	2100
20	$HV_{OUT}113$	0	2210
21	$HV_{OUT}112$	0	2320
22	$HV_{OUT}111$	0	2430
23	$HV_{OUT}110$	0	2540
24	$HV_{OUT}109$	0	2650
25	$HV_{OUT}108$	0	2760
26	$HV_{OUT}107$	0	2870
27	$HV_{OUT}106$	0	2980
28	$HV_{OUT}105$	0	3090
29	$HV_{OUT}104$	0	3200
30	$HV_{OUT}103$	0	3310
31	$HV_{OUT}102$	0	3420
32	$HV_{OUT}101$	0	3530
33	$HV_{OUT}100$	0	3640
34	$HV_{OUT}99$	0	3750
35	$HV_{OUT}98$	0	3860
36	$HV_{OUT}97$	0	3970
37	$HV_{OUT}96$	0	4080
38	$HV_{OUT}95$	0	4190
39	$HV_{OUT}94$	0	4300
40	$HV_{OUT}93$	0	4410
41	$HV_{OUT}92$	0	4520
42	$HV_{OUT}91$	0	4630
43	$HV_{OUT}90$	0	4740
44	$HV_{OUT}89$	0	4850
45	$HV_{OUT}88$	0	4960
46	$HV_{OUT}87$	0	5070
47	$HV_{OUT}86$	0	5180
48	$HV_{OUT}85$	0	5290
49	$HV_{OUT}84$	0	5400
50	$HV_{OUT}83$	0	5510
51	$HV_{OUT}82$	0	5620
52	$HV_{OUT}81$	0	5730
53	$HV_{OUT}80$	0	5840
54	$HV_{OUT}79$	0	5950
55	$HV_{OUT}78$	0	6060
56	$HV_{OUT}77$	0	6170
57	$HV_{OUT}76$	0	6280
58	$HV_{OUT}75$	0	6390
59	$HV_{OUT}74$	0	6500
60	$HV_{OUT}73$	0	6610

Pad #	Name	X	Y
61	$HV_{OUT}72$	0	6720
62	$HV_{OUT}71$	0	6830
63	$HV_{OUT}70$	0	6940
64	$HV_{OUT}69$	0	7050
65	$HV_{OUT}68$	0	7160
66	$HV_{OUT}67$	0	7270
67	$HV_{OUT}66$	0	7380
68	$HV_{OUT}65$	0	7490
69	$HV_{OUT}64$	0	7600
70	V_{PP}	263.1	7963.5
71	V_{PP}	373.1	7963.5
72	PGND	607.1	7802.5
73	PGND	717.1	7802.5
74	V_{PP}	977.1	7963.5
75	V_{PP}	1087.1	7963.5
76	PGND	1347.1	7802.5
77	PGND	1457.1	7802.5
78	V_{PP}	1691.1	7963.5
79	V_{PP}	1801.1	7963.5
80	$HV_{OUT}63$	2064.2	7600
81	$HV_{OUT}62$	2064.2	7490
82	$HV_{OUT}61$	2064.2	7380
83	$HV_{OUT}60$	2064.2	7270
84	$HV_{OUT}59$	2064.2	7160
85	$HV_{OUT}58$	2064.2	7050
86	$HV_{OUT}57$	2064.2	6940
87	$HV_{OUT}56$	2064.2	6830
88	$HV_{OUT}55$	2064.2	6720
89	$HV_{OUT}54$	2064.2	6610
90	$HV_{OUT}53$	2064.2	6500
91	$HV_{OUT}52$	2064.2	6390
92	$HV_{OUT}51$	2064.2	6280
93	$HV_{OUT}50$	2064.2	6170
94	$HV_{OUT}49$	2064.2	6060
95	$HV_{OUT}48$	2064.2	5950
96	$HV_{OUT}47$	2064.2	5840
97	$HV_{OUT}46$	2064.2	5730
98	$HV_{OUT}45$	2064.2	5620
99	$HV_{OUT}44$	2064.2	5510
100	$HV_{OUT}43$	2064.2	5400
101	$HV_{OUT}42$	2064.2	5290
102	$HV_{OUT}41$	2064.2	5180
103	$HV_{OUT}40$	2064.2	5070
104	$HV_{OUT}39$	2064.2	4960
105	$HV_{OUT}38$	2064.2	4850
106	$HV_{OUT}37$	2064.2	4740
107	$HV_{OUT}36$	2064.2	4630
108	$HV_{OUT}35$	2064.2	4520
109	$HV_{OUT}34$	2064.2	4410
110	$HV_{OUT}33$	2064.2	4300
111	$HV_{OUT}32$	2064.2	4190
112	$HV_{OUT}31$	2064.2	4080
113	$HV_{OUT}30$	2064.2	3970
114	$HV_{OUT}29$	2064.2	3860
115	$HV_{OUT}28$	2064.2	3750
116	$HV_{OUT}27$	2064.2	3640
117	$HV_{OUT}26$	2064.2	3530
118	$HV_{OUT}25$	2064.2	3420
119	$HV_{OUT}24$	2064.2	3310
120	$HV_{OUT}23$	2064.2	3200

Pad #	Name	X	Y
121	$HV_{OUT}22$	2064.2	3090
122	$HV_{OUT}21$	2064.2	2980
123	$HV_{OUT}20$	2064.2	2870
124	$HV_{OUT}19$	2064.2	2760
125	$HV_{OUT}18$	2064.2	2650
126	$HV_{OUT}17$	2064.2	2540
127	$HV_{OUT}16$	2064.2	2430
128	$HV_{OUT}15$	2064.2	2320
129	$HV_{OUT}14$	2064.2	2210
130	$HV_{OUT}13$	2064.2	2100
131	$HV_{OUT}12$	2064.2	1990
132	$HV_{OUT}11$	2064.2	1880
133	$HV_{OUT}10$	2064.2	1770
134	$HV_{OUT}9$	2064.2	1660
135	$HV_{OUT}8$	2064.2	1550
136	$HV_{OUT}7$	2064.2	1440
137	$HV_{OUT}6$	2064.2	1330
138	$HV_{OUT}5$	2064.2	1220
139	$HV_{OUT}4$	2064.2	1110
140	$HV_{OUT}3$	2064.2	1000
141	$HV_{OUT}2$	2064.2	890
142	$HV_{OUT}1$	2064.2	780
143	$HV_{OUT}0$	2064.2	670
144	V_{PP}	2064.2	520
145	V_{PP}	2064.2	410
146	PGND	2064.2	260
147	PGND	2064.2	150
148	DGND	2064.2	0
149	D_{1B}	1940.2	-210.1
150	D_{2B}	1825.5	-210.1
151	D_{3B}	1710.8	-210.1
152	D_{4B}	1596.1	-210.1
153	CLK	1481.5	-210.1
154	LE	1366.8	-210.1
155	RST	1252.1	-210.1
156	DGND	1142.1	-210.1
157	DIR	1032.1	-210.1
158	V_{DD}	922.1	-210.1
159	$\overline{OE}$	812.1	-210.1
160	$\overline{OH}$	697.4	-210.1
161	$\overline{OL}$	582.7	-210.1
162	D_{4A}	468	-210.1
163	D_{3A}	355.3	-210.1
164	D_{2A}	238.6	-210.1
165	D_{1A}	123.9	-210.1

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